Design of Delta-Sigma ΣΔ based Fractional N PLL Frequency Synthesizer for GSM Mobile Systems

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Abstract

This paper presents the design of Delta-Sigma ΣΔ based fractional N PLL frequency synthesizer for GSM mobile systems. The loop filter is one of main element in fractional-N ΣΔ synthesizer because it shapes the noise spectrum of quantization error and reduce the spurious level in the pass band of PLL. The effect of loop filter order is studied and it is shown that by increasing the order of the loop filter, the phase noise performance will be improved, although this requires careful design consideration, as the PLL is prone instability. It's shown that the 3rd order loop filter and 3rd order ΣΔ modulator gives the best performance with reducing phase noise (13dBc/Hz) and spurious noise (44dBc) of the output signal.

Keyword: PLL, Frequency Synthesizer, ΣΔ Modulator, Fractional-N, GSM mobile systems.

تصميم مركب التردد المسند لدوائر إقفال الطور الجزئية للنظام الخلوي

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الخلاصة

تناول هذا البحث تصميم ومحاكاة مركب التردد المسند لدوائر اقفال الطور الجزئية لاستخدامه في أنظمة الاتصالات الخلوية. حيث يعبر مرشح الدورة من العناصر الرئيسية لدوائر مركب التردد لانه يشكل طيف الضوضاء الناتج عن خطأ التكميم ويقلل من الضوضاء النبضية في PLL. حيث بينت النتائج ان زيادة درجة مرشح الدورة يحسن ضوضاء الطور ويحتاج الى عناية في التصميم لكي لا تصبح الدائرة غير مستقرة, كذلك تبين النتائج ان مرشح الدورة من المرتبة الثالثة هو الافضل من حيث تقليل ضوضاء الطور وزمن الخطأ حيث أعطى التصميم المقترح تحسينا واضحا من ناحية ضوضاء الطور(13dBc/Hz) وضوضاء النبضة (44dBc).

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1. Introduction

Oscillators and frequency synthesizers are key elements in a radio system that provide a controlled frequency source for received signal down conversion and for transmitted signal up conversion. A stand-alone oscillator or a voltage controlled oscillator (VCO) does not have the required frequency stability to satisfy the low phase noise requirement. Therefore frequency synthesis is necessary to obtain accurate high frequencies from a precise low frequency crystal oscillator [1].

Scott E. Meninger designed the fractional N synthesizer with 1st order loop filter and 1st ΣΔ modulator at 3.6GHz [2]. The Charlotte Y. Lau designed the fractional N synthesizer using direct closed loop realization algorithm at third order ΣΔ [3]. In this paper using PLL Design Assistance Program (PDA) to designed the loop filter with 2nd and 3rd order and the ΣΔ modulator is chosen to be of the 1st to 5th order in order to select a best performance.

Frequency mixing utilizes a mixer to multiply two signals together, generating a signal that contains both the sum and the difference of the two input frequencies as shown in Fig(1). Typically, only one of these two frequencies is required. This type of synthesizer has very good noise performance and the same stability as the reference oscillator. Frequency mixing is accomplished by using a nonlinear element such as a diode or a transistor.

Unfortunately, the non-linearity's tend to produce a signal that contains many spurious tones at various mixing products and the final signal will be a combination of many frequencies with the from $nf_a \pm mf_b$ where the f_a and f_b are, respectively input frequency and mixed frequency and n&m are integer number. These spurious frequencies are the basic disadvantage of frequency mixing [4].

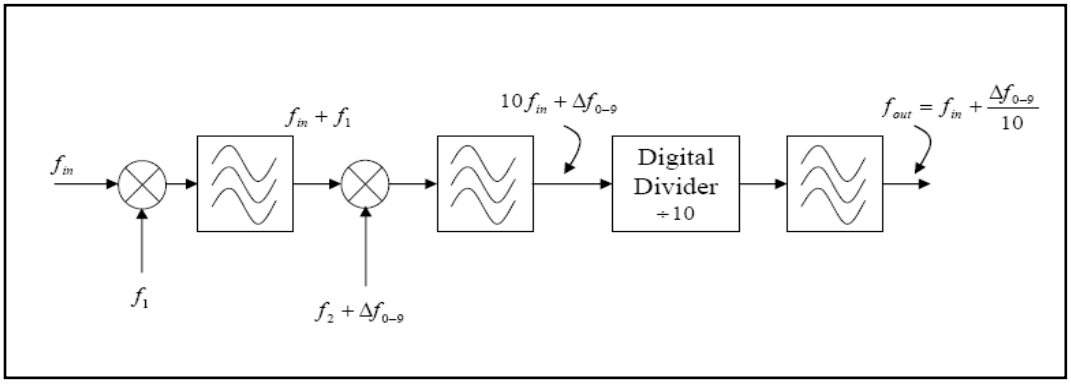

Fig. 1 Frequency synthesis using frequency mixing method

Phase locked loops (PLL) are often used to provide negative feedback in frequency synthesizers to suppress the phase noise due to oscillators.

The fractional-N technique modifies the classical indirect phase-locked loops to effectively permit the feedback divider to take a periodically changing division ratio and hence to give a non-integer ratio. For instance, if a fractional value of 1/8 is required, then the division ratio changes once (from N to N+ 1) every eighth cycle.

The architecture of a fractional-N synthesizer is shown in Fig(2) , the accumulator is a convenient device to control the division ratio because the number of occurrences of its carry-out equals the numerator of the fraction [4].

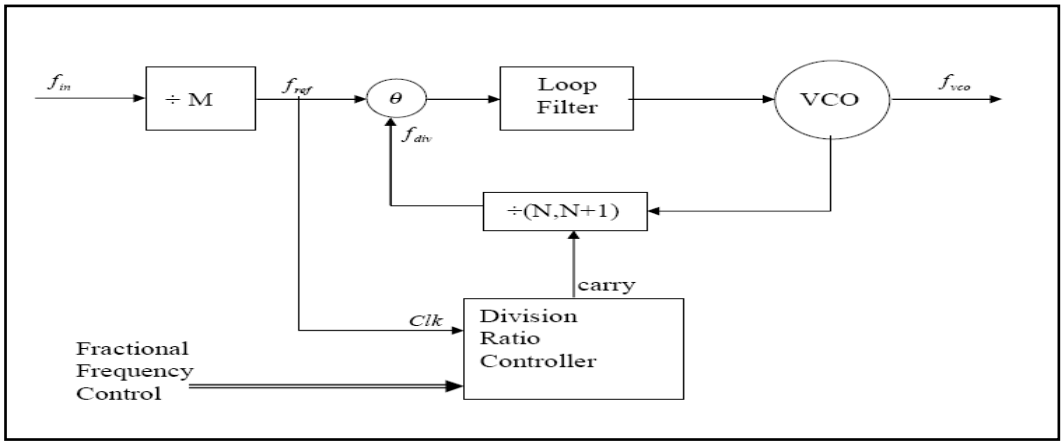

Fig. 2 Conventional fractional-N synthesizer

The manipulation of the division ratio in Fig(2) generates phase perturbations, and hence spurious signals, which have to be eliminated in the synthesizer. The nature of the phase perturbations is predictable and can be canceled out using an analogue correction system. If the VCO output frequency is now changed from $N.f_{ref}$ to $(N.g).f_{ref}$ while maintaining the feedback division ratio as N, the phase detector phase error takes on a sawtooth shape in Fig(3)[2,4,5] is given by

$$\frac{\Delta\theta}{\Delta T}=\left(\frac{N+0.g}{N}\right)f_{ref}.T\left(\frac{2\pi}{T}\right)-f_{ref}T\left(\frac{2\pi}{T}\right) \qquad \text{---------- (1)}$$

$$\frac{\Delta\theta}{\Delta T}=\left(\frac{2\pi\ f_{ref}\,0.g}{N}\right)\bmod 2\pi \qquad \text{---------- (2)}$$

where 0.g denotes the fractional portion of the division ratio**,** T is the time of one period.

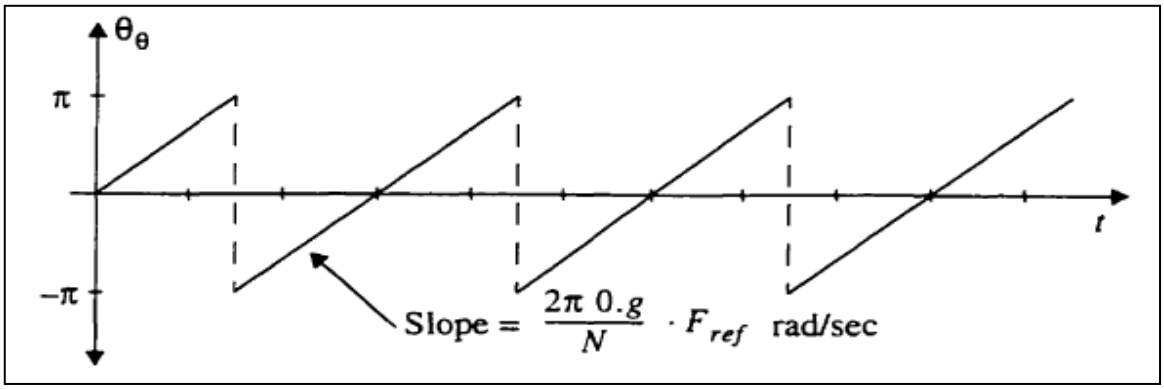

Fig. 3 Beat note from the output of the phase detector

2.The proposed System

Fig(4) shows fractional-N synthesizer with high speed phase selection [2,3,6]. It is proposed that the loop filter is to be designed with 2nd and 3rd order in order to examined the synthesizer for best performance, also the ΣΔ modulator is to be examined with the order variation from 1st to the 5th. The overall system with variable loop filter order and variable ΣΔ modulator is tested in order to reduce the phase noise, spurious noise and the r.m.s jitter time.

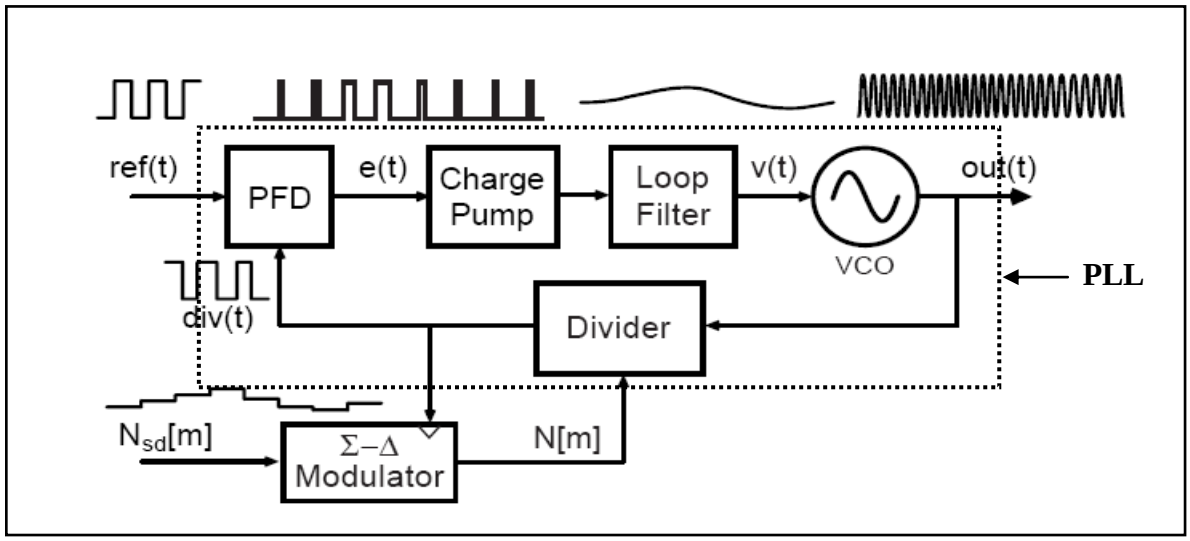

Fig. 4 The proposed ΣΔ fractional-N synthesizer

As shown in Fig(4),the PLL still acts as a digitally-controlled frequency generator, the phase modulator produces a bit stream, N[m], that contains the desired frequency control embedded in a stream of binary number. The average density of binary numbers controls the division ratio of the PLL and hence the output frequency of the synthesizer [5]. The phase modulator will tend to shape the noise spectrum of the quantization error and reduce spurious level in the PLL output signal [1,4].

3. Simulation Result

A Fractional-N PLL frequency synthesizer for GSM900 receiver applications with a frequency range of 880 MHz to 915 MHz, a channel spacing of 1MHz, and a settling time of less(10 μsec) is targeted, where the reference frequency (f_{ref}) is 25 MHz [3,6,8].

Typically, a higher-order loop filter is used in Fractional-N PLL frequency synthesis applications to provide adequate suppression of the reference spurious, the high frequency phase noise from the ΣΔ modulator, can be eliminated by using high order loop filter.

The charge pump loop filter topology is a third-order passive network as shown in Fig(5). The use of a higher-order loop filter, however, requires careful design consideration, i.e., passive component must be determined theoretically. Therefore, its precision values must be implement in hardware, as the PLL is prone to instability. The average current-to-voltage transfer function of the loop filter is [6,8].

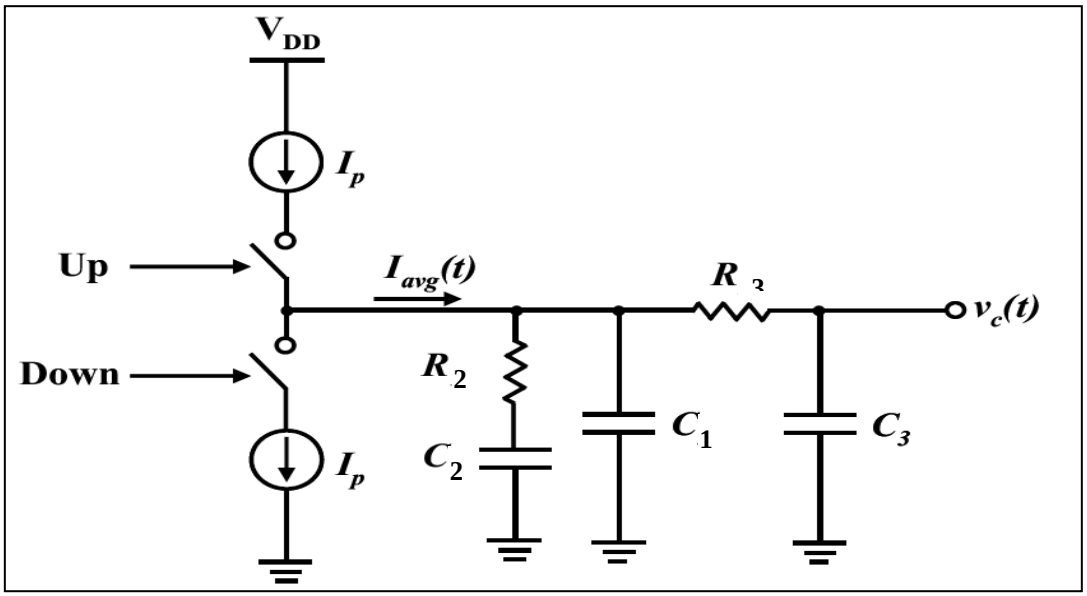

Fig. 5 A passive third-order charge pump loop filter

$$H(s) = \frac{(1+s\tau_2)}{A_0 \quad s(1+s\tau_1)(1+s\tau_3)} \qquad ...(3)$$

$$H(s) = \frac{1+s\tau_2}{s(A_2 s^2 + A_1 s + A_o)} \qquad ...(4)$$

$$A_0 = \frac{Kv.I_{cp}.\alpha}{K\,N_{norm}} \qquad ...(5)$$

where
Nnom : Nominal divide value,
Kv : VCO gain, (units are assumed to be Hz/V),
α : PFD topology,
Icp : Charge pump current,. (units assumed to be Amps)
K: PFD constant, ,(units assumed to be Amps/rad)

$\tau_2 = R_2 C_2$
$A_o = C_1 + C_2 + C_3$
$A_1 = A_o(\tau_1 + \tau_3) = C_2C_3R_2 + C_1C_2R_2 + C_1C_3R_3 + C_2C_3R_3$
$A_2 = A_o(\tau_1\tau_3) = C_1C_2R_2C_3R_3$

The open loop transfer function of the PLL can be determined from the following expression [6,9].

$$A(s) = \frac{K_v I_{cp} \alpha H(s)}{s\ N_{norm}} \qquad ...(6)$$

Where N_{norm} is the geometric mean of the maximum and minimum division ratio required to span the desired frequency band (in this case,36).

$$N_{norm} = \frac{f_{out}}{f_{ref.}} \qquad ...(7)$$

Where

f_{out}:output frequency equal to 900MHz .

Using PLL Design Assistance Program (PDA) and Matlab 7.4 the calculated coefficients of the 3rd order loop filter are

C_1=4.1952nf, C_2=0.34474nf, C_3=0.52669nf, R_2=379.373ohm, R_3=197.3867ohm I_{cp}=2mA, K=2.193x10^{12}Amp/rad and K_v=200MHz/volt.

With these passive component values, the open loop transfer function of the PLL is displayed in Fig (6), where the unity gain frequency is 8.97MHz and the phase margin is(48.4°). This value of phase margin (48.4°) can be expressed as optimum value (more than 45° and less than 90°) that gives the best stability for the system [8].
Using the parameters which are calculated in the previous section, the fractional-N PLL frequency synthesizer is simulated using Sue2 program [7].

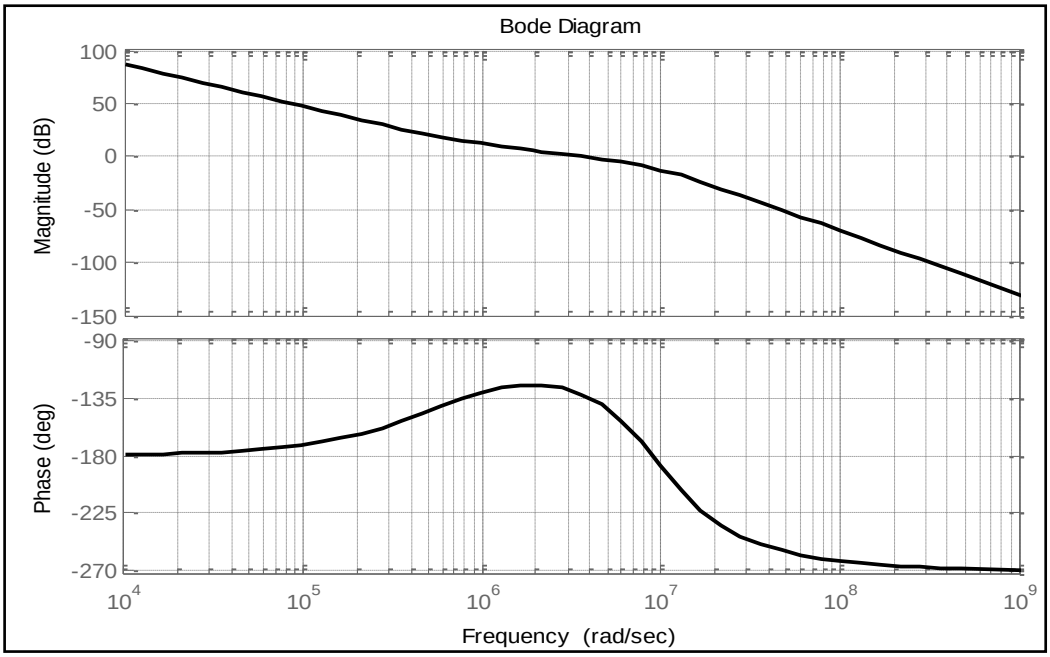

Fig. 6 Open loop transfer function of the PLL

The relationship between ΣΔ modulator and r.m.s jitter output is shown in Fig(7). It is clear that the 3rd order give less jitter noise compared with 1st and 2nd order, the small deference between 4th ,5th is equal (0.9pico sec).

The ΣΔ modulator at 3rd order multi-stage-noise-shaping (MASH) is designed according to the following equation [7].

$$NTF = \frac{Y(z)}{R(z)} = (1 - 3z^{-1} + 3z^{-2} - z^{-3}) \qquad ...(8)$$

Where NTF is noise transfer function.
The step response of the closed the loop PLL system that used in the fractional-N ΣΔ frequency synthesizer is shown in Fig(8),it is clear that the settling time is very small and is equal to (5μ sec)

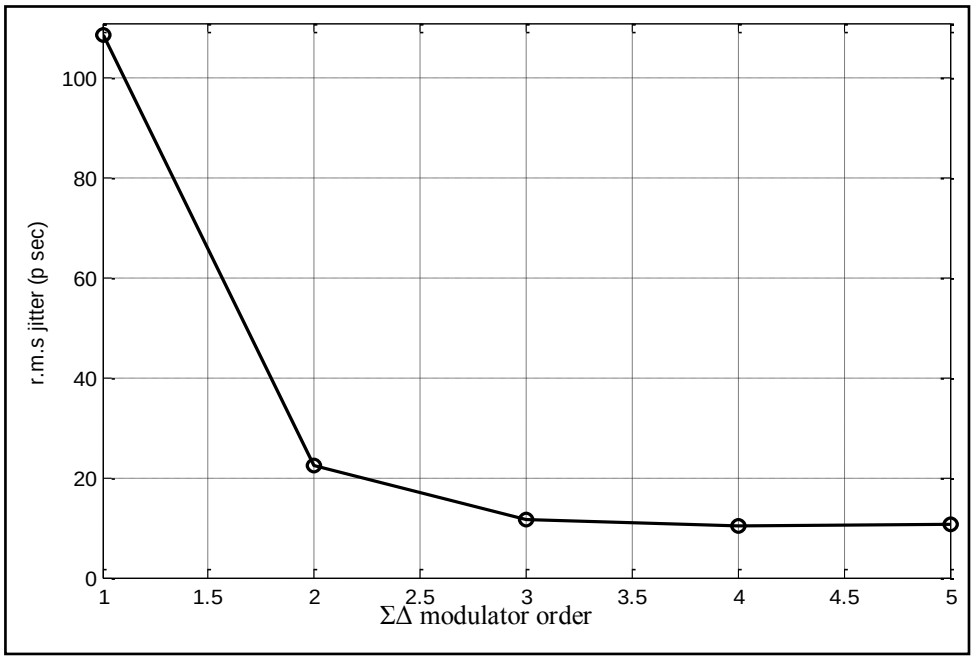

Fig. 7 Relationship between r.m.s jitter with order of ΣΔ modulator MASH

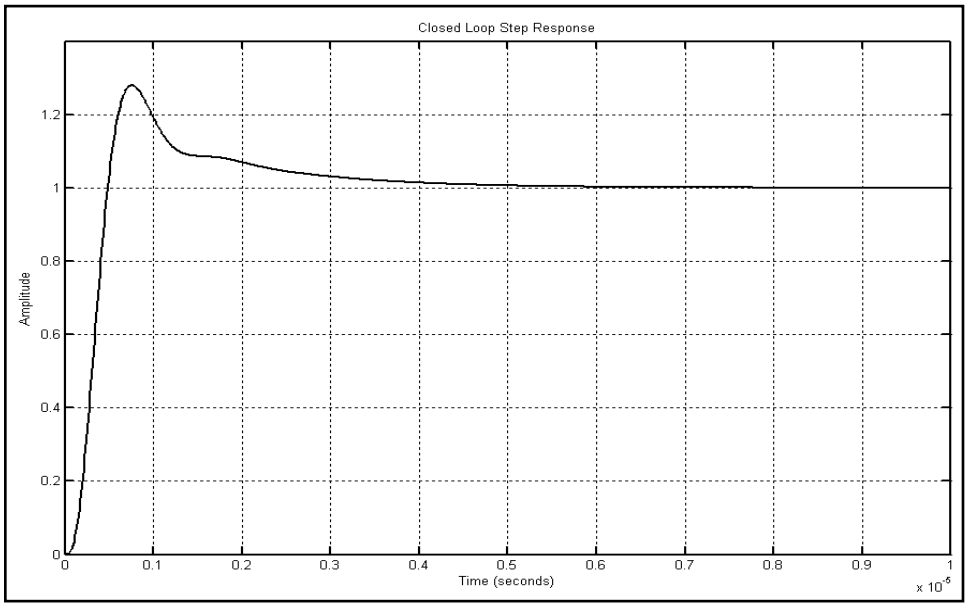

Fig. 8 Step response of PLL 3rd order

The GSM phase noise values (L(f)) as a function of frequency offset is shown

In Fig (9) and Fig(10). The phase noise is equal to (-140dBc/Hz) and the spurious noise is equal to (50dBc) at frequency offset 20MHz using 3rd order ΣΔ modulator MASH and 2nd order loop filter as shown in Fig(9). While, as shown in Fig(10), the phase noise is equal to(-153dBc/Hz) and the spurious noise is equal to (6dBc) at frequency offset 20MHz using 3rd order ΣΔ modulator and 3rd order loop filter.

As shown in Fig(10) it can be seen that use of 3rd order loop filter improves the phase noise of about (13dBc/Hz) and also improves the spurious noise of about (44dBc). The comparison of the proposed system with prior works is shown in Table (1).

In the present work, the value of phase noise is smaller than the value in references [2] and [3]. Also the spurious noise is reduced by amount of 4dBc compared to reference [2]. The settling time and r.m.s jitter time are also reduced to value of 5μs and 11ps, respectively.

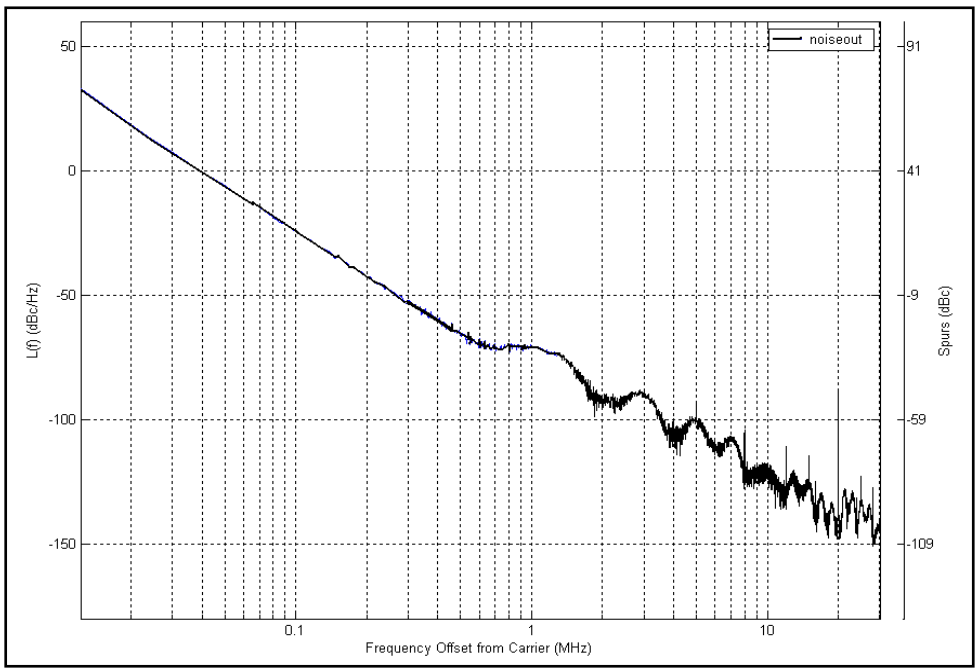

Fig. 9 Phase noise level with frequency offset for 3rd order ΣΔ modulator MASH

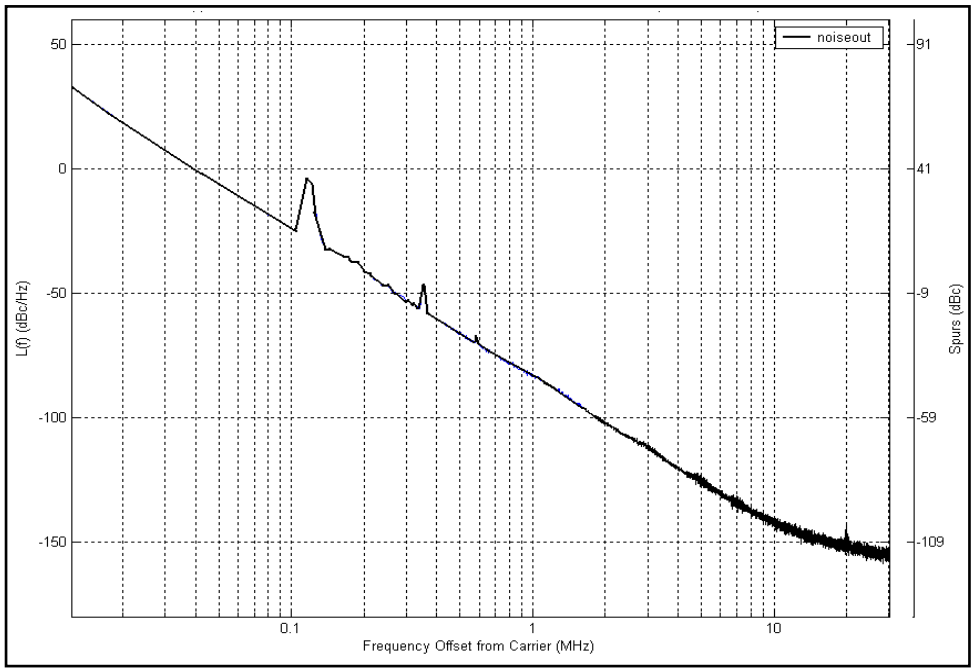

Fig. 10 Phase noise level with frequency offset for 3rd order ΣΔ modulator MASH

Table (1): Comparison with prior works.

The parameter	[2]	[3]	Present work
Bandwidth	1MHZ	300KHz	1MHz
Loop filter order	1st order	3rd order	2nd and 3rd order
ΣΔ modulator order	1st order MASH	3rd order	1st -5th order MASH
phase noise at frequency offset 10MHz	-141dBc/Hz	-143dBc/Hz	-145dBc/Hz
Spurious noise at frequency offset 20MHz	10dBc	not calculated	6dBc
Jitter time	not calculated	14.055ps	11ps
Settling time for PLL	not calculated	10µs	5µs

4.Conclusion

The fractional-N ΣΔ modulator frequency synthesizer has been simulated using Matlab ,PDA and Sue2 programs. The result has shows that increasing the order of the ΣΔ modulator from 1st to 5th order will improve the spurious noise performance, and the best order is the 3rd one because it gives minimum r.m.s jitter. While increasing the order of loop filter will improve the phase noise performance and reduce the spurious noise. The open loop transfer function and the close loop transfer function prove that the system is stable because the phase margin is greater than 45 and less than 90.In this paper a considerable improvement was achieved in minimizing spurious noise level, r.m.s jitter time and settling time compared with published papers in this domain.

5. References

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